

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1 1-8. (Cancelled)

1 9. (Previously Presented) An apparatus, comprising:

2 a storage structure to store at least one entry, the at least one entry to include a
3 register identifier value;

4 a first physical rename register of a first length;

5 a second physical rename register of a second length different than the first
6 length, wherein the first and second rename registers are distinct from each other and
7 do not share any common bits;

8 a logical predicate register; and

9 rename logic to map an instance of the logical predicate register to a selected
10 physical rename register, where the selected physical rename register is selected from
11 a plurality of registers comprising the first physical rename register and the second
12 physical rename register;

1 wherein the register identifier value is to indicate a current length, wherein the
2 current length is selected from a set including the first length and the second length;

3 wherein the logical register includes a plurality of x bit positions;
1 wherein a selected one of the x bit positions may be accessed individually
2 responsive to a first instruction that indicates the selected bit position;
3 wherein all x bit positions may be accessed together responsive to a second
4 instruction; and
5 the rename logic is further to allocate the first physical rename register
6 responsive to the first instruction, the rename logic further to allocate the second
7 physical rename register responsive to the second instruction.

1 10. (Previously Presented) The apparatus of claim 9, wherein:

2 a subset including y of the x bits may be accessed responsive to a third
3 instruction, where $y > 1$; and
4 the rename logic is further to allocate the first physical rename register
5 responsive to the third instruction.

1 11. (Original) The apparatus of claim 10, wherein:

2 the length of the first physical rename register includes y bit positions.

1 12. (Original) The apparatus of claim 11, wherein:

2 the entry is further to include a position identifier, the position identifier to indicate
3 a selected one of the y bit positions of the first physical rename register.

1 13. (Original) The apparatus of claim 12, wherein:
2 the selected one of the y bit positions of the first physical rename register
3 corresponds to the selected bit position indicated by the first instruction.

1 14. (Previously Presented) A method comprising:
2 determining that a current instruction indicates as a destination register a
3 multiple-bit-field (MBF) predicate register having n bit positions, where $n > 1$; and
4 allocating a physical rename register for the destination register;
5 wherein allocating further comprises allocating a physical rename register of a
6 first length responsive to the current instruction indicating a partial-bit write of only 1 bit
7 position of the MBF predicate register and further comprises allocating a physical
8 rename register of a second length responsive to the current instruction indicating a
9 bulk-bit write of x bit positions of the predicate register, where x is greater than 1 and x
10 is less than or equal to n.

1 15. (Original) The method of claim 14, wherein:
2 allocating further comprises modifying a rename map table to indicate the
3 allocated physical rename register.

1 16. (Previously Presented) The method of claim 14, wherein:

2 the allocating further includes allocating a physical rename register of the first
3 length responsive to the current instruction indicating a partial-bit write of y bit positions
4 of the predicate register, where $1 < y < x$.

1 17. (Previously Presented) The method of claim 16, wherein:

2 the y bit positions are contiguous.

1 18. (Original) The method of claim 14, wherein:

2 the x bit positions are contiguous.

1 19. (Previously Presented) The method of claim 14, wherein:

2 the allocating further comprises allocating a physical rename register of the
3 second length responsive to the current instruction indicating a bulk-bit write of all n bit
4 positions of the predicate register.

1 20. (Original) The method of claim 16, wherein:

2 $y=2$.

1 21. (Original) The method of claim 16, wherein:

2 $y=4$.

- 1 22. (Original) The method of claim 14, further comprising:
- 2 modifying the current instruction to indicate the allocated physical rename
- 3 register in place of the MBF register.

- 1 23-30. (Cancelled)